CLAIMS

What is claimed is:

1. A radio receiver comprises:

low noise amplifier operably coupled to amplify a radio frequency (RF) signal to produce an amplified RF signal;

intermediate frequency (IF) mixing module operably coupled to mix the amplified RF signal with a local oscillation to produce a digital IF signal; and

digital demodulator that includes:

mixing section operably coupled to produce a digital I signal and a digital Q signal from the digital IF signal;

first digital comb filter operably coupled to filter the digital I signal to produce a filtered I signal;

second digital comb filter operably coupled to filter the digital Q signal to produce a filtered Q signal;

phase locked loop module operably coupled to produce a digital signal based on the filtered I signal and the filtered Q signal; and

data recovery module operably coupled to produce a data stream from the digital signal.

2. The radio receiver of claim 1, wherein each of the first and second digital comb filters further comprises:

frequency response having notches at frequencies that substantially correspond with frequencies of interfering channel frequencies of the RF signal.

3. The radio receiver of claim 1, wherein each of the first and second digital comb filters further comprises a cascaded integrated comb filter.

4. The radio receiver of claim 1, wherein the mixing section further comprises:

state machine operably coupled to frequency shift by a factor of N and phase shift by π/2 the digital IF signal to produce the digital I signal and to frequency shift by the factor of N and phase shift by -π the digital IF signal to produce the digital Q signal.

5. The radio receiver of claim 1, wherein the mixing section further comprises:

direct digital frequency synthesizer to produce the digital I signal and the digital Q signal from the digital IF signal.

6. The radio receiver of claim 1, wherein the IF mixing module further comprises:

local oscillation generation operably coupled to produce the local oscillation to have a Q local oscillation and an I local oscillation;

I mixer operably coupled to mix the amplified RF signal with the I local oscillation to produce an IF I signal;

Q mixer operably coupled to mix the amplified RF signal with the Q local oscillation to produce an IF Q signal;

band pass filter operably ccupled to band pass filter the IF I and IF Q signals to prcduce a filtered IF signal;

limiter operably coupled to limit magnitude of the filtered IF signal to produce limited IF signal; and

analog to digital converter operably coupled to convert the limited IF signal into the digital IF signal.

7. The radio receiver of claim 1, wherein the phase locked loop module further comprises:

phase locked loop (PLL) operably coupled to produce a PLL signal based on the filtered I and Q signals;

low pass filter/equalizer operably coupled to equalize and low pass filter the PLL signal to produce an equalized and filtered digital signal.

8. A radio receiver comprises:

low noise amplifier operably coupled to amplify a radio frequency (RF) signal to produce an amplified RF signal;

intermediate frequency (IF) mixing module operably coupled to mix the amplified RF signal with a local oscillation to produce a digital IF signal; and

digital demodulator that includes:

mixing section operably coupled to mix the digital IF signal with a reference I signal and a reference Q signal to produce a digital I signal and a digital Q signal;

phase locked loop module operably coupled to produce a digital signal based on the digital I signal and the digital Q signal; and

data recovery module operably coupled to receive the digital signal, wherein the data recovery module includes:

DC offset module cperably coupled to receive the digital signal and to determine a DC offset using a first criteria during an acquisition mode and to determined the DC offset using second criteria during a tracking mode, wherein the DC offset module substantially removes the DC offset from the digital signal to produce a DC adjusted digital signal; and

data extraction module operably coupled to sample the DC adjusted digital signal at a sample rate to produce a data stream.

9. The radio receiver of claim 8, wherein the data recovery module further comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

determine, on a packet by packet basis, the acquisition mode and the tracking mode.

10. The radio receiver of claim 9, wherein the memory further comprises operational instructions that cause the processing module to:

determine a peak value of the digital signal based on at least one of: current peak value, a previous peak value, and the first or second criteria;

determine a valley value of the digital signal based on at least one of: current valley value, a previous valley value, and the first or second criteria; and

determine the DC offset based the peak value and the valley value.

11. The radio receiver of claim 10, wherein the memory further comprises operational instructions that cause the processing module to determine the peak value by:

determine whether magnitude of the current peak value is greater than magnitude of the previous peak value;

when the magnitude of the current peak value is greater than the magnitude of the previous peak value, store the current peak value as the peak value; and

when the magnitude of the current peak value is not greater than the magnitude of the previous peak value, determine the peak value as a result of the previous peak value less a peak acquisition delta value multiplied by a difference of the current peak value and the previous peak value, wherein the first criteria indicates a greater value for the peak acquisition delta value than the second criteria.

12. The radio receiver of claim 10, wherein the memory further comprises operational instructions that cause the processing module to determine the valley value by:

determine whether absolute value of a magnitude of the current valley value is greater than absolute value of a magnitude of the valley peak value;

when the absolute value of the magnitude of the current valley value is greater than the absolute value of the magnitude of the previous valley value, store the current valley value as the valley value; and

when the absolute value of the magnitude of the current valley value is not greater than the absolute value of the magnitude of the previous valley value, determine the valley value as a result of the previous valley value plus a valley acquisition delta value multiplied by a difference of the current valley value and the previous valley value, wherein the first criteria indicates a greater value for the valley acquisition delta value than the second criteria.

13. The radio receiver of claim 10, wherein the memory further comprises operational instructions that cause the processing module to detect false peaks and false valleys by:

detect a potential peak of the digital signal;

determine magnitude of the potential peak;

determine a difference between the magnitude of the potential peak and magnitude of the valley value;

when the difference is less than a predetermined value, indicate that the potential peak is a false peak;

detect a potential valley of the digital signal;

determine magnitude of the potential valley;

determine a second difference between the magnitude of the potential valley and magnitude of the peak value; and

when the second difference is less than the predetermined value, indicate that the potential valley is a false valley.

14. The radio receiver of claim 10, wherein the memory further comprises operational instructions that cause the processing module to detect peaks and valleys by:

determine a gradient of the digital signal;

determine when the gradient changes for positive to negative;

indicate the digital signal as being at a peak when the gradient changes from positive to negative;

determine when the gradient changes for negative to positive; and

indicate the digital signal as being at a valley when the gradient changes from positive to negative.

15. The radio receiver of claim 9, wherein the phase locked loop module further comprises:

phase locked loop (PLL) operably coupled to produce a PLL signal based on the filtered I and Q signals;

tapped delay line operably coupled to delay the PLL signal based on a delay signal to produce a delayed PLL signal; and

low pass filter/equalizer operably coupled to equalize and low pass filter the delayed PLL signal to produce the digital signal.

16. The radio receiver of claim 15, wherein the memory further comprises operational instructions that cause the processing module to:

obtain a first reference sample prior to the sample of the DC adjusted digital signal;

obtain a second reference sample subsequent to the sample of the DC adjusted digital signal;

accumulate, over a plurality of samples of the DC adjusted digital signal, a difference between the first and second reference samples to produce an accumulated difference; and

adjust the delay signal to provide less delay when the accumulated difference overflows an upper threshold and to provide more delay when the accumulated difference underflows a lower threshold.

17. The radio receiver of claim 9, wherein the memory further comprises operational instructions that cause the processing module to:

over-sample the DC adjusted digital signal at the sample rate to produce a plurality of samples per bit;

correlate alternate ones of the plurality of samples over a plurality of bits corresponding to a synchronization word of a packet of the DC adjusted digital signal to produce a plurality of correlated sample sets;

identify one of the plurality of correlated sample sets as having a best-correlation with the synchronization word to produce an identified correlated sample set;

select a sampling position of the over-sampling of the DC adjusted digital signal based on the identified correlated sample set to produce a selected sample position; and

utilize samples at the selected sample position to produce the data stream.

18. The radio receiver of claim 17, wherein the memory further comprises operational instructions that cause the processing module to select the sampling position by:

compare adjacent ones of the plurality of correlated sample sets to the identified correlated sample set with respect to typical waveform of the DC adjusted digital signal to determine an over-sampling relationship of the DC adjusted digital signal;

select the sampling position to be the sampling that produces the identified correlated sample set when the sampling that produces the identified correlated sample set occurs at a most favorable point of the over-sampling relationship; and

select the sampling position to be a sampling between the identified correlated sample set and an adjacent one of the plurality of correlated sample sets when the sampling between the identified correlated sample set and an adjacent one of the plurality of correlated sample sets occurs at a most favorable point of the over-sampling relationship.

19. A radio receiver comprises:

low noise amplifier operably coupled to amplify a radio frequency (RF) signal to prcduce an amplified RF signal;

intermediate frequency (IF) mixing module operably coupled to mix the amplified RF signal with a local oscillation to produce a digital IF signal; and

digital demodulator that includes:

mixing section operably coupled to mix the digital IF signal with a reference I signal and a reference Q signal to produce a digital I signal and a digital Q signal;

phase locked loop operably coupled to produce a digital signal based on the digital I signal and the digital Q signal;

low pass filter/equalizer module operably coupled to the phased locked loop to equalize and low pass filter the digital signal to produce an equalized and filtered signal;

data recovery module operably coupled to produce a data stream from the filtered digital signal.

20. The radio receiver of claim 19, wherein the low pass filter/equalizer further comprises:

digital logic circuit to provide a zero at approximately baseband.

21. The radio receiver of claim 19, wherein the low pass filter/equalizer further comprises:

first digital comb filter that has a frequency response having notches at frequencies that substantially correspond with frequencies of interfering channel frequencies of the RF signal; and

second digital comb filter that has a frequency response having notches at frequencies that substantially correspond with image frequencies of at least one of the mixing section and the IF mixing module.

22. The radio receiver of claim 19, wherein the low pass filter/equalizer module further comprises:

frequency step down module operably coupled to reduce frequency of the filtered digital signal.

23. A radio receiver comprises:

low noise amplifier operably coupled to amplify a radio frequency (RF) signal to prcduce an amplified RF signal;

intermediate frequency (IF) mixing module operably coupled to mix the amplified RF signal with a local oscillation to produce an IF I signal and an IF Q signal;

polyphase filter operably ccupled to filter the IF I and Q signals and to provide image rejection of the location oscillation to produce a filtered I signal and a filtered Q signal;

limiting module operably coupled to limit magnitude of the filtered I signal to produce a limited I signal;

analog to digital converter operably coupled to convert the limited I signal into a digital I signal; and

digital demodulator that includes:

mixing section operably coupled to mix the digital I signal with a reference I signal and a reference Q signal to produce a digital baseband I signal and a digital baseband Q signal;

phase locked loop module operably coupled to produce a digital signal based on the digital baseband I signal and the digital baseband Q signal; and

data recovery module operably coupled to produce a data stream from the digital signal.

24. The radio receiver of claim 23, wherein the mixing section further comprises:

first digital comb filter operably coupled to filter a product of the mixing of the digital I signal with the reference I signal to produce the digital baseband I signal;

second digital comb filter cperably coupled to filter a product of the mixing of the digital Q signal with the reference Q signal to produce the digital baseband Q signal.

25. The radio receiver of claim 24, wherein the mixing section further comprises:

state machine operably coupled to frequency shift by a factor of N and phase shift by π/2 the digital I signal to produce the product of the mixing of the digital I signal with the reference I signal and to frequency shift by the factor of N and phase shift by -π the digital I signal to produce the product of the mixing of the digital Q signal with the reference Q signal.

26. The radio receiver of claim 23, wherein the data recovery module further comprises:

DC offset module operably ccupled to receive the digital signal and to determine a DC offset using a first criteria

during an acquisition mode and to determined the DC offset using second criteria during a tracking mode, wherein the DC offset module substantially removes the DC offset from the digital signal to produce a DC adjusted digital signal; and

data extraction module operably coupled to sample the DC adjusted digital signal at a sample rate to produce a data stream.

27. The radio receiver of claim 23, wherein the digital demodulator further comprises:

low pass filter/equalizer mcdule operably coupled between the phased locked loop and the data recovery module, wherein the low pass filter/equalizer equalize and low pass filter the digital signal tc produce an equalized and filtered digital signal.

28. A method for receiving a radio frequency (RF) signal, the method comprises:

amplifying the RF signal to produce an amplified RF signal;

mixing the amplified RF signal with a local oscillation to produce a digital IF signal;

producing a digital Q signal and a digital I signal from a synthesized frequency and the digital IF signal;

comb filtering the digital I signal to produce a filtered I signal;

comb filtering the digital Q signal to produce a filtered Q signal;

generating a digital signal based on the filtered I signal and the filtered Q signal via a phase locked loop function; and

producing a data stream from the digital signal.

29. The method of claim 28, wherein the comb filtering the digital I and Q signals further comprises:

filtering frequencies that substantially correspond with frequencies of interfering channel frequencies of the RF signal and passing other frequencies.

30. The method of claim 28, wherein the producing the digital I and Q signals further comprises:

shifting frequency by a factor of N and phase by π/2 of the digital IF signal to produce the digital I signal; and

shifting frequency by the factor of N and phase by -π of the digital IF signal to prcduce the digital Q signal.

31. The method of claim 28, wherein the mixing the amplified RF signal with the local oscillation further comprises:

generating the local oscillation to have a Q local oscillation and an I local cscillation;

mixing the amplified RF signal with the I local oscillation to produce an IF I signal;

mixing the amplified RF signal with the Q local oscillation to produce an IF Q signal;

band pass filtering the IF I and Q signals to produce a filtered IF signal;

limiting magnitude of the filtered IF signal to produce limited IF signal; and

converting the limited IF signal into the digital IF signal.

32. The method of claim 28, wherein the generating the digital signal further comprises:

producing a phase locked locp (PLL) signal based on the filtered I and Q signals; and

equalizing and low pass filtering the PLL signal to produce an equalized and filtered signal.

33. A method for data detection, the method comprises:

receiving a digital signal;

determining a DC offset using a first criteria during an acquisition mode and using second criteria during a tracking mode;

substantially removing the DC offset from the digital signal to produce a DC adjusted digital signal; and

sampling the DC adjusted digital signal at a sample rate to produce a data stream.

34. The method of claim 33 further comprises:

determining, on a packet by packet basis, the acquisition mode and the tracking mode.

35. The method of claim 33, wherein the determining the DC offset further comprises:

determining a peak value of the digital signal based on a current peak value, a previcus peak value, and the first or second criteria;

determining a valley value cf the digital signal based on a current valley value, a previous valley value, and the first or second criteria; and

determining the DC offset based the peak value and the valley value.

36. The method of claim 35, wherein the determining the peak value further comprises:

determining whether magnitude of the current peak value is greater than magnitude of the previous peak value;

when the magnitude of the current peak value is greater than the magnitude of the previous peak value, storing the current peak value as the peak value; and

when the magnitude of the current peak value is not greater than the magnitude of the previous peak value, determining the peak value as a result of the previous peak value less a peak acquisition delta value multiplied by a difference of the current peak value and the previous peak value, wherein the first criteria indicates a greater value for the peak acquisition delta value than the second criteria.

37. The method of claim 35, wherein the determine the valley value further comprises:

determining whether absolute value of a magnitude of the current valley value is greater than absolute value of a magnitude of the valley peak value;

when the absolute value of the magnitude of the current valley value is greater than the absolute value of the magnitude of the previous valley value, storing the current valley value as the valley value; and

when the absolute value of the magnitude of the current valley value is not greater than the absolute value of the magnitude of the previous valley value, determining the valley value as a result of the previous valley value plus a valley acquisition delta value multiplied by a difference of the current valley value and the previous valley value, wherein the first criteria indicates a greater value for the valley acquisition delta value than the second criteria.

38. The method of claim 35 further comprises detecting false peaks and false valleys by:

detecting a potential peak cf the digital signal;

determining magnitude of the potential peak;

determining a difference between the magnitude of the potential peak and magnitude of the valley value;

when the difference is less than a predetermined value, indicating that the potential peak is a false peak;

detecting a potential valley of the digital signal;

determining magnitude of the potential valley;

determining a second difference between the magnitude of the potential valley and magnitude of the peak value; and

when the second difference is less than the predetermined value, indicating that the potential valley is a false valley.

39. The method of claim 35 further comprises detecting peaks and valleys by:

determining a gradient of the digital signal;

determining when the gradient changes for positive to negative;

indicating the digital signal as being at a peak when the gradient changes from positive to negative;

determining when the gradient changes for negative to positive; and

indicating the digital signal as being at a valley when the gradient changes from positive to negative.

40. The method of claim 33 further comprises:

obtaining a first reference sample prior to the sampling of the DC adjusted digital signal;

obtaining a second reference sample subsequent to the sampling of the DC adjusted digital signal;

accumulating, over a plurality of samples of the DC adjusted digital signal, a difference between the first and

second reference samples to produce an accumulated difference; and

adjusting the sampling when the accumulated difference overflows an upper threshold or when the accumulated difference underflows a lower threshold.

41. The method of claim 33, wherein the sampling the DC adjusted digital signal further comprises:

over-sampling the DC adjusted digital signal at the sample rate to produce a plurality of samples per bit;

correlating alternate ones of the plurality of samples over a plurality of bits corresponding to a synchronization word of a packet of the DC adjusted digital signal to produce a plurality of correlated sample sets;

identifying one of the plurality of correlated sample sets as having a best-correlation with the synchronization word to produce an identified correlated sample set;

selecting a sampling position of the over-sampling of the DC adjusted digital signal based on the identified correlated sample set to produce a selected sample position; and

utilizing samples at the selected sample position to produce the data stream.

42. The method of claim 41, wherein the selecting the sampling position further comprises:

comparing adjacent ones of the plurality of correlated sample sets to the identified correlated sample set with respect to typical waveform of the DC adjusted digital signal to determine an over-sampling relationship of the DC adjusted digital signal;

selecting the sampling position to be the sampling that produces the identified correlated sample set when the sampling that produces the identified correlated sample set occurs at a most favorable point of the over-sampling relationship; and

selecting the sampling position to be a sampling between the identified correlated sample set and an adjacent one of the plurality of correlated sample sets when the sampling between the identified correlated sample set and an adjacent one of the plurality of correlated sample sets occurs at a most favorable point of the over-sampling relationship.

43. A method for receiving a radio frequency (RF) signal, the method comprises:

amplifying the RF signal to produce an amplified RF signal;

mixing the amplified RF signal with a local oscillation to produce a digital IF signal;

mixing the digital IF signal with a reference I signal and a reference Q signal to produce a digital I signal and a digital Q signal;

producing a digital signal based on the digital I signal and the digital Q signal using a phase locked loop function;

equalizing and low pass filtering the digital signal to produce an equalized and filtered digital signal; and

producing a data stream from the filtered digital signal.

44. The method of claim 43, wherein the equalizing and low pass filtering the digital signal further comprises:

filtering, with a zero at approximately baseband, the digital signal.

45. The method of claim 43, wherein the equalizing and low pass filtering further comprises:

filtering frequencies that substantially correspond with frequencies of interfering channel frequencies of the RF signal and passing other frequencies; and

filtering frequencies that substantially correspond with image frequencies of at least one of: the mixing the amplified RF signal with the local oscillation and the mixing the digital IF signal with the reference I signal and the reference Q signal.

46. The method of claim 43 further comprises:

reducing frequency of the filtered digital signal.

47. An apparatus for receiving a radio frequency (RF) signal, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operaticnal instructions that cause the processing module to:

amplify the RF signal to prcduce an amplified RF signal;

mix the amplified RF signal with a local oscillation to produce a digital IF signal;

produce a digital Q signal and a digital I signal from a synthesized frequency and the digital IF signal;

comb filter the digital I signal to produce a filtered I signal;

comb filter the digital Q signal to produce a filtered Q signal;

generate a digital signal based on the filtered I signal and the filtered Q signal via a phase locked loop function; and

produce a data stream from the digital signal.

48. The apparatus of claim 47, wherein the memory further comprises operational instructions that cause the

processing module to comb filter the digital I and Q signals by:

filtering frequencies that substantially correspond with frequencies of interfering channel frequencies of the RF signal and passing other frequencies.

49. The apparatus of claim 47, wherein the memory further comprises operational instructions that cause the processing module to produce the digital I and Q signals by:

shifting frequency by a factor of N and phase by π/2 of the digital IF signal to produce the digital I signal; and

shifting frequency by the factor of N and phase by -π of the digital IF signal to prcduce the digital Q signal.

50. The apparatus of claim 47, wherein the memory further comprises operational instructions that cause the processing module to mix the amplified RF signal with the local oscillation by:

generating the local oscillation to have a Q local oscillation and an I local cscillation;

mixing the amplified RF signal with the I local oscillation to produce an IF I signal;

mixing the amplified RF signal with the Q local oscillation to produce an IF Q signal;

band pass filtering the IF I signal and the IF Q signal to produce a filtered I signal and a filtered Q signal, respectively;

limiting magnitude of the filtered I and Q signals to produce limited I and Q signals; and

converting the limited I and Q signals into the digital IF signal.

51. The apparatus of claim 47, wherein the memory further comprises operational instructions that cause the processing module to generate the digital signal by:

producing a phase locked loop (PLL) signal based on the filtered I and Q signals; and

equalizing and low pass filtering the PLL signal to produce an equalized and filtered digital signal.

52. An apparatus for data detection, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operaticnal instructions that cause the processing module to:

receive a digital signal;

determine a DC offset using a first criteria during an acquisition mode and using second criteria during a tracking mode;

substantially remove the DC offset from the digital signal to produce a DC adjusted digital signal; and

sample the DC adjusted digital signal at a sample rate to produce a data stream.

53. The apparatus of claim 52, wherein the memory further comprises operational instructions that cause the processing module to:

determine, on a packet by packet basis, the acquisition mode and the tracking mode.

54. The apparatus of claim 52, wherein the memory further comprises operational instructions that cause the processing module to determine the DC offset by:

determining a peak value of the digital signal based on a current peak value, a previcus peak value, and the first or second criteria;

determine a valley value of the digital signal based on a current valley value, a previous valley value, and the first or second criteria; and

determine the DC offset based the peak value and the valley value.

55. The apparatus of claim 54, wherein the memory further comprises operational instructions that cause the processing module to determine the peak value by:

determining whether magnitude of the current peak value is greater than magnitude of the previous peak value;

when the magnitude of the current peak value is greater than the magnitude of the previous peak value, storing the current peak value as the peak value; and

when the magnitude of the current peak value is not greater than the magnitude of the previous peak value, determining the peak value as a result cf the previous peak value less a peak acquisition delta value multiplied by a difference of the current peak value and the previous peak value, wherein the first criteria indicates a greater value for the peak acquisition delta value than the second criteria.

56. The apparatus of claim 54, wherein the memory further comprises operational instructions that cause the processing module to determine the valley value by:

determining whether absolute value of a magnitude of the current valley value is greater than absolute value of a magnitude of the valley peak value;

when the absolute value of the magnitude of the current valley value is greater than the absolute value of the magnitude of the previous valley value, storing the current valley value as the valley value; and

when the absolute value of the magnitude of the current valley value is not greater than the absolute value of the magnitude of the previous valley value, determining the valley value as a result of the previous valley value plus a valley acquisition delta value multiplied by a difference of the current valley value and the previous valley value, wherein the first criteria indicates a greater value for the valley acquisition delta value than the second criteria.

57. The apparatus of claim 54, wherein the memory further comprises operational instructions that cause the processing module to detect false peaks and false valleys by:

detecting a potential peak cf the digital signal;

determining magnitude of the potential peak;

determining a difference between the magnitude of the potential peak and magnitude of the valley value;

when the difference is less than a predetermined value, indicating that the potential peak is a false peak;

detecting a potential valley of the digital signal;

determining magnitude of the potential valley;

determining a second difference between the magnitude of the potential valley and magnitude of the peak value; and

when the second difference is less than the predetermined value, indicating that the potential valley is a false valley.

58. The apparatus of claim 52, wherein the memory further comprises operational instructions that cause the processing module to detect peaks and valleys by:

determining a gradient of the digital signal;

determining when the gradient changes for positive to negative;

indicating the digital signal as being at a peak when the gradient changes from positive to negative;

determining when the gradient changes for negative to positive; and

indicating the digital signal as being at a valley when the gradient changes from positive to negative.

59. The apparatus of claim 52, wherein the memory further comprises operational instructions that cause the processing module to:

obtain a first reference sample prior to the sampling of the DC adjusted digital signal;

obtain a second reference sample subsequent to the sampling of the DC adjusted digital signal;

accumulate, over a plurality of samples of the DC adjusted digital signal, a difference between the first and second reference samples to produce an accumulated difference; and

adjust the sampling when the accumulated difference overflows an upper threshold or when the accumulated difference underflows a lower threshold.

60. The apparatus of claim 52, wherein the memory further comprises operational instructions that cause the processing module to sampling the DC adjusted digital signal by:

over-sampling the DC adjusted digital signal at the sample rate to produce a plurality of samples per bit;

correlating alternate ones of the plurality of samples over a plurality of bits corresponding to a synchronization word

of a packet of the DC adjusted digital signal to produce a plurality of correlated sample sets;

identifying one of the plurality of correlated sample sets as having a best-correlation with the synchronization word to produce an identified correlated sample set;

selecting a sampling position of the over-sampling of the DC adjusted digital signal based on the identified correlated sample set to produce a selected sample position; and

utilizing samples at the selected sample position to produce the data stream.

61. The apparatus of claim 60, wherein the memory further comprises operational instructions that cause the processing module to select the sampling position by:

comparing adjacent ones of the plurality of correlated sample sets to the identified correlated sample set with respect to typical waveform of the DC adjusted digital signal to determine an over-sampling relationship of the DC adjusted digital signal;

selecting the sampling position to be the sampling that produces the identified correlated sample set when the sampling that produces the identified correlated sample set occurs at a most favorable point of the over-sampling relationship; and

selecting the sampling position to be a sampling between the identified correlated sample set and an adjacent one of the plurality of correlated sample sets when the sampling between the identified correlated sample set and an adjacent one of the plurality of correlated sample sets occurs at a most favorable point of the over-sampling relationship.

62. An apparatus for receiving a radio frequency (RF) signal, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operaticnal instructions that cause the processing module to:

amplify the RF signal to prcduce an amplified RF signal;

mix the amplified RF signal with a local oscillation to produce a digital IF signal;

mix the digital IF signal with a reference I signal and a reference Q signal to produce a digital I signal and a digital Q signal;

produce a digital signal based on the digital I signal and the digital Q signal using a phase locked loop function;

equalize and filter the digital signal to produce an equalized and filtered signal; and

produce a data stream from the filtered digital signal.

63. The apparatus of claim 62, wherein the memory further comprises operational instructions that cause the processing module to equalize the digital signal by:

filtering, with a zero at approximately baseband, the digital signal to produce the equalized signal.

64. The apparatus of claim 62, wherein the memory further comprises operational instructions that cause the processing module to comb filter the equalized signal by:

filtering frequencies that substantially correspond with frequencies of interfering channel frequencies of the RF signal and passing other frequencies; and

filtering frequencies that substantially correspond with image frequencies of at least one of: the mixing the amplified RF signal with the local oscillation and the mixing the digital IF signal with the reference I signal and the reference Q signal.

65. The apparatus of claim 62, wherein the memory further comprises operational instructions that cause the processing module to:

reduce frequency of the filtered digital signal.